Specification Amendments

Please replace paragraph 001 with the following re-written paragraph:

001 This invention generally relates to metal-insulator-metal structures and more particularly to an MIM structure and method for depositing plasma enhanced oxide ~~deposition~~ to achieve a MIM capacitor structure with improved capacitance reliability.

Please replace paragraph 003 with the following re-written paragraph:

003 One immediate problem with the integration of analog and digital circuitry blocks is the increase in power consumption. The design constraints that inform the design of digital blocks include the need for fast signal transmission and low power consumption. On the other hand in analog circuitry, as device sizes have decreased, the power supply to the circuitry has been decreased, leading to susceptibility of a signal to noise levels in the circuitry. As a result, a differential signal is frequently used including a local Vdd boost to decrease

sensitivity to thermal noise.

Please replace paragraph 0013 with the following re-written paragraph:

0013 Figure 2 is a cross-sectional view of a portion of an exemplary MIM semiconductor structure at a further processing stage according to the present invention.

Please replace paragraph 0015 with the following re-written paragraph:

0015 The method and MIM capacitor structure according to the present invention is more clearly described by referring to Figures 1A - 1E where cross sectional views at stages of manufacture are shown in forming an MIM capacitor structure.

Please replace paragraph 0018 with the following re-written paragraph:

0018 In a preferred embodiment, the bottom electrode 16 includes a lower layer of Ta 16A with an overlying layer of TaN 16B as an uppermost portion which is preferably silicided to form TaSiN deposited by conventional methods, for example PVD deposition of Ta followed by deposition of TaN layer 16B by an ion metal plasma (IMP) process, followed by plasma enhanced silicidation, using a silane, or chlorosilane source, for example disilane, or dichlorosilane, to treat the TaN layer. The thickness of the bottom electrode 16 may range from about 500 Angstroms to about 1500 Angstroms.

Please replace paragraph 0025 with the following re-written paragraph:

0025 According to the present invention, the beneficial effect of the SRO sandwiching layers in reducing or preventing interdiffusion between the PECVD oxide layer and the electrodes is believed to be related to the relatively higher density of the SRO layers, as evidenced by the refractive index, compared to the

PECVD oxide layer as well as the increased presence of nitrogen in the SiO_2 lattice to thereby inhibiting lattice diffusion across the SRO layer interface. In addition, it has been found that silicidation of the electrode layer surface, for example TaN to form TaSiN together with an adjacent intervening SRO layer between the electrode and PECVD layer further improves a resistance to interfacial diffusion, believed to be due to the higher atomic binding energy of ~~Ti~~ Ta to Si. As a result, the MIM structure can reproducibly achieve design capacitances with closer tolerances while forming more stable and reliable MIM structures. In addition, electronic matching of capacitance components with other electronic components in a mixed mode system, especially for smaller design technologies including to 0.13 microns and below is improved thereby improving overall device operability.

Please replace paragraph 0026 with the following re-written paragraph:

0026 Referring to Figure 2, an exemplary MIM structure is completed by, conventional photolithographical patterning and RIE

etching to form the upper and bottom portions 24A and 24B, for example by a first etch process stopping on the USG layer 14 and a second etch process stopping on the PE Oxide layer 18B, respectively. Next, an overlying dielectric insulating layer 26 is deposited. Dual or single Damascene interconnects are then patterned and RIE etched by conventional processes followed by filling with metal, for example copper by an electro-chemical plating process, to form copper electrodes 28A, 28B and copper landing interconnects (e.g. vias) 30A, 30B, 30C.